Digital PM Demodulator for Brazilian Data Collecting System

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ABSTRACT
This paper presents the project and implementation results of a digital PM demodulator system for processing LEO satellite signals from Brazilian Data Collecting System. The demodulator was implemented on the Altera Cyclone II DSP Development Kit equipped with FPGA EP2C70. Demodulation is done with a second order Digital Phase Locked Loop (DPLL) with $-\pi$ to π linear phase detector realized by a CORDIC algorithm operating on vectoring mode. The parameters of the DPLL were calculated using control system theory.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Style– *algorithms implemented in hardware.* B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids. B.4.1 [**Input/Output and Data Communication**]: Data Communication Devices – *processors.*

General Terms
Algorithms, Design, Experimentation, Theory.

Keywords
phase locked loop (PLL), BDCS, FPGA, control system theory.

1. INTRODUCTION
Low Earth Orbit (LEO) satellite signals experiences phase acceleration due to the Doppler Effect [1]. Thus, in order to demodulate these signals a synchronization system that can track signal with phase acceleration is required. Although second order Phase Locked Loop (PLL) cannot achieve zero phase error while tracking a signal that experiences phase acceleration, it is possible to decrease the steady state error to acceptable values by adjusting its gains, and with that avoid a complicated third order PLL project.

Digital PLL (DPLL) is widely used to perform demodulation. Integrated circuits with DPLLs, such as the HSP5020 [7], and articles on DPLL projects [2] are easy to find. In this paper we present a digital PM demodulator for LEO satellites from Brazilian Data Collecting System (BDCS) using a second order Digital PLL (DPLL), implemented on a Field Programmable Gate Array (FPGA). To increase the lock range of the DPLL we use $-\pi$ to $+\pi$ linear phase detector. For this, we use Costas Loop architecture with cartesian to polar converter realized by a COordinate Rotation Digital Computer (CORDIC) algorithm operating on vectoring mode.

BDCS has more than 600 Data Collector Platforms (DCP) spreaded over the country, most of them using weather sensors. They transmit a signal to 3 LEO satellites: CBERS2, SCD1, and SCD2. The satellites modulate the signals from the DCPs and transmit the modulated signal to ground stations, where the data is recovered and sent to the mission center in Cachoeira Paulista to be distributed to the system's users.

The main advantage of the proposed digital demodulator for BDCS over the fully analog existent ones is the reconfiguration capacity of FPGA. This provides flexibility to the ground stations.

2. BDCS SIGNAL PROCESSING SYSTEM
The satellite signal is a 1.8 rad Phase Modulation (PM) with a carrier frequency of about 2.2 GHz and a base band of 65 kHz to 125 kHz. The maximum Doppler acceleration is 750 Hz/s and the maximum Doppler shift is ±60 kHz [6]. In order to recover the DCP signals, the ground station uses a down converter followed by a PM demodulator. After this, each DCP signal must be detected and processed to retrieve the transmitted data [6].

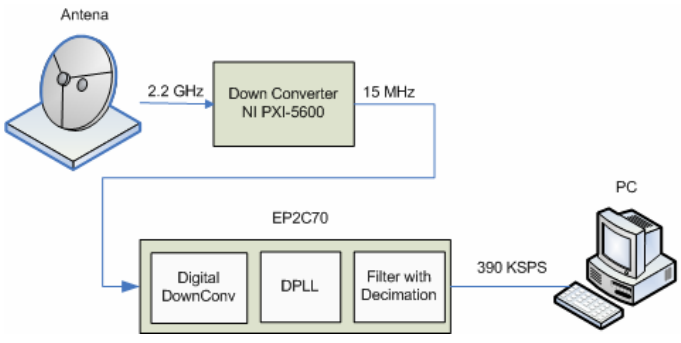

Figure 1. Ground Station Signal Processing System for Brazilian Data Collecting System.

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Figure 1 shows the project of the signal processing system of EMM-Natal ground station where the proposed digital PM demodulator will be implemented. The PM demodulation will be implemented on the EP2C70 FPGA. A personal computer (PC) will be used for further signal processing of the recovered DCP signals by software.

Equipped with the EP2C70 FPGA, a high performance A/D and D/A converter, output/input pins, and one 100 MHz onboard clock, Cyclone II EP2C70 DSP Development Kit has all the components necessary to implement the digital demodulator. Table 1 shows important characteristics of the kit for this application.

Table 1. Cyclone II DSP Development Kit Characteristics

Component	Characteristics
EP2C70	68416 Logical Elements 150 18x18 or 300 9x9 Embedded Multipliers 250 MK4 blocks – 1152 KRAM bits
A/D	2.2 VPP, 12 bit, 120 MSPS, 70 dB SNR

3. DIGITAL DOWNCONVETER

The IF signal from the analog downconverter NI PXI-5600 is centered at 15 MHz and has a passband of 20 MHz. The internal A/D converter from the Cyclone II DSP Development Kit operates synchronized with a 100 MHz on-board clock, so that the digitalized signal has a sample rate of 100 Mega Sample per Second (MSPS).

To improve the demodulator performance we introduced, in the FPGA, a digital downconverter centered in 15 MHz, with cut-off frequency 195 kHz, and decimation of 16. The cut-off frequency is a little bigger than the base band signal plus the maximum frequency deviation caused by the Doppler Effect ($125 + 60 = 185\ kHz$), resulting in maximum noise attenuation. The decimation´s main purpose is to allow lowpass filtering with FIR Filter without using too many taps. The signal is also divided in two components, the in-phase and quadrature. This is necessary because the DPLL that makes the PM demodulation operates with complex input. The digital downconverter was implemented using the architecture shown in fig. 2. Software "FIR Compiler" from Altera was used to generate the filters and estimate the number of consumed Logical Elements (LE's) for the configuration that we used.

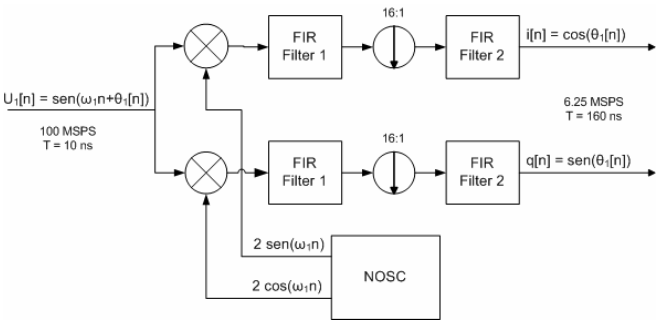


Figure 2. Digital Downconverter.

4. DIGITAL PLL PROJECT

The project of a second order digital PLL can be done by designing the transfer function of a continuous-time PLL and mapping their poles to the discrete-time domain [2]. A common method used to design a second order continuous-time PLL is to find the damping factor (ξ) and the natural frequency (ω_n) using equations that relate them to the project specifications.

Equation (1) below is the transfer function between phase input and error of a second order PLL with a PI Loop Filter. The equation is written as function of the damping factor (ξ) and the natural frequency (ω_n) parameters:

$$H_E(S) = \frac{E(s)}{\Theta_1(s)} = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (1)$$

Figure. 3 shows the block diagram of the linear model of the implemented DPLL. The structured was based on the zero-order holder conversion from the continuous-time PLL with a PI Loop Filter [3]. Equation (2) is its transfer function between the phase input and the error.

$$H_E(z) = \frac{E(z)}{\theta_1(z)} = \frac{(1 - z^{-1})^2}{1 + (K_P - 2)z^{-1} + (1 + K_I - K_P)z^{-2}} \quad (2)$$

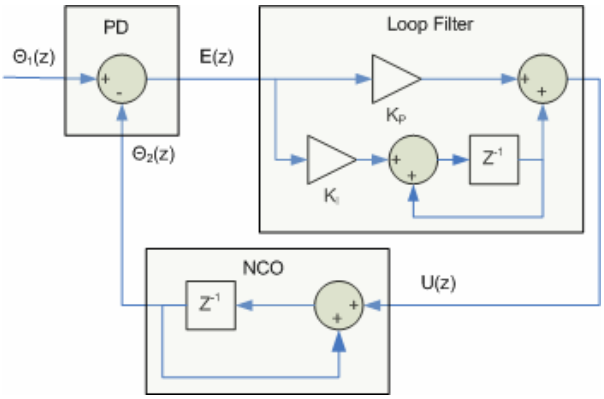


Figure 3. Linear model of the digital phase locked loop.

It is desired that the PLL frequency response be narrow to minimize the lock error due to noise, but not too much, otherwise the search process becomes too slow and even a pull-in limit can exist due to the limited precision of the NCO. So it was decided to use the damping factor (ξ) that resulted in narrowest transition band and specified a minimum lock range to calculate ω_n.

Making $s = j\omega$ and normalizing the frequency to the natural frequency ($\omega = X \cdot \omega_n$), we have the frequency response between $\Theta_1(z)$ and E(z):

$$H_E(X) = \frac{-X^2}{(1 - X^2) + j(2\xi X)} \quad (3)$$

Analyzing Fig. 4 where $|H_E(X)|$ are shown for different ξ, we verify that narrowest transition band is achieved with:

$$\xi = 0.707 \quad (4)$$

In [3] the lock range for a second order PLL that uses a –π to π linear phase detector is given below.

$$\Delta\omega_{Lock} \approx 2\pi\xi\omega_n \tag{5}$$

Thus for a lock range of 40 kHz we obtain:

$$\omega_n = 5.66\cdot 10^4\ rad/s = 9\ kHz \tag{6}$$

Since the PLL has no dynamic to follow the modulation, $|H_E(\omega_m)| \approx 1$, where ω_m is the lowest limit of the base band signal (65 kHz), the demodulation signal will appear in the error signal.

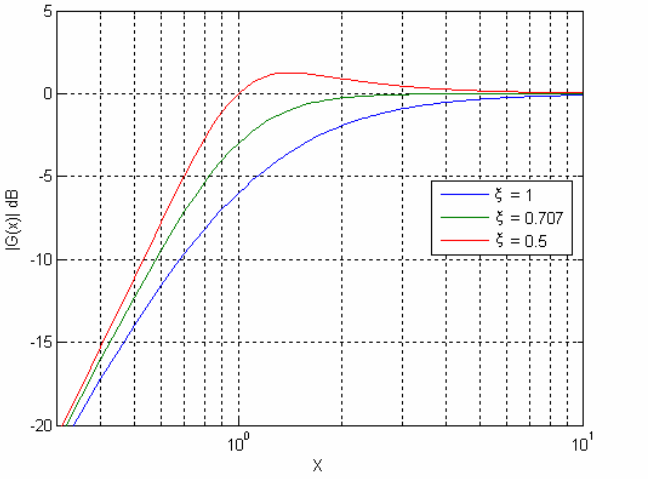


Figure 4. Magnitude of G(X) for some ξ ≤1.

After the damping factor and natural frequency were calculated, we relate them with the Digital PLL gains K_P and K_I by mapping the poles from the continuous to the discrete time domain. Finally, we must check if the steady-state phase error due to Doppler acceleration is small enough to be ignored, and check the system's stability.

4.1 Mapping the Poles

Mapping the poles from (1) to the standard second order discrete transfer function [2] presented below:

$$H(z) = \frac{N(z)}{z^2 + C_1 z + C_0} \tag{7}$$

$$C_1 = -2\,e^{-\xi\omega_n T}\cos(\omega_n T\sqrt{1-\xi^2}) \tag{8}$$

$$C_0 = e^{-2\xi\omega_n T} \tag{9}$$

Where T is the sample period 160ns. This results because of the digital down converter decimation of 16 over the 100 MSPS signal from the A/D converter. Comparing (2) with (7) we get:

$$C_1 = K_P - 2 \tag{10}$$

$$C_0 = 1 - K_P + K_I \tag{11}$$

Using equations (8), (9), (10) and (11) we find the solution for K_P and K_I.

$$K_P = 2 - 2\,e^{-\xi\omega_n T}\cos(\omega_n T\sqrt{1-\xi^2}) \tag{12}$$

$$K_I = 1 - 2\,e^{-\xi\omega_n T}\cos(\omega_n T\sqrt{1-\xi^2}) + e^{-2\xi\omega_n T} \tag{13}$$

Substituting (4) and (6) in (12) and (13) we calculate K_P and K_I:

$$K_P = 1.28\cdot 10^{-2} \tag{14}$$

$$K_I = 8.14\cdot 10^{-5} \tag{15}$$

4.2 Steady-State Phase Error

LEO satellites signals experiences a phase acceleration (*R*) caused by the Doppler Effect. For BDCS signal this acceleration can reach $R_{\max} = 2\pi\cdot 750 rad/s^2$. Using (2) and supposing $\theta_1(t) = \frac{R_{\max}}{2}t^2$, we can calculate the maximal steady-state phase error caused by this acceleration. Appling zero order holder and z transform to $\theta_1(t)$.

$$\theta_1(z) = R_{\max}T^2\frac{z^{-1}}{(1-z^{-1})^3}$$

According to the Final-Value Theorem, the steady-state error is:

$$\lim_{z^{-1}\to 1}(1-z^{-1})E(z) = \frac{R_{\max}T^2}{K_I} = 1.48\cdot 10^{-6} rad$$

With this result we make sure that the steady-state phase error is very small and can be ignored.

4.3 Stability

According to control theory a discrete system is stable if all poles of its transfer function are inside the unit circle |z| = 1. The resultant poles from our loop are $0.9936 \pm j\cdot 0.0064$. The absolute value of these poles is 0.9936, so the system is stable.

5. DIGITAL PLL IMPLEMENTATION

Figure 5 shows the architecture used in the DPLL. The Numerical Controlled Oscillator (NCO) was implemented with the aid of the software "NCO Compiler" from Altera, which generates the VHDL code, and estimates the resources, according to the specified parameters. The Cartesian-Polar converter was implemented using the CORDIC vectoring mode algorithm, with an asynchronous architecture, including a first rotation of –π/2 or π/2 rad to increase it operation range to –π to +π rad. This CORDIC architecture can be seen in [5]. The Loop Filter was implemented as presented in fig. 3, with the only difference that saturation was included in the accumulator to limit the frequency tracking between $\pm 6.14\cdot 10^5 rad/s$.

The output sample rate of 6.25 MSPS is still too high to be processed in real time by the PC that will do further signal processing. Then a digital low pass filter with cut-off frequency 150 kHz and decimation of 16 was introduced at the DPLL output

(error signal), resulting in output sample rate for the PC of 391 KSPS.

VHDL language was used for all the blocks, and software Quartus II was used to compile and program the device. Table 2 and 3 show the parameters of the NCO and Cartesian-Polar Converter. The full project, composed by the digital downconverter, the DPLL, and the output filter, consumed 25% of the logical elements and 20% of the memory RAM available in the EP2C70.

Table 2. NCO PARAMETERS

Architecture	Large ROM
Accumulator precision	30 bits
Phase precision	12 bits
Magnitude precision	12 bits
Clock	6.25 MHz
Number of LE's	73
MK4	48

Table 3. CORDIC Parameters

Architecture	Asynchrony
Number of Layer	12
Phase precision	16 bits
X and Y precision	12 bits
Number of LE's	1.510
Max t_{pd}	57.42 ns (17.42 MHz)

6. SIMULATION RESULTS

The simulations were made using DSP Builder toolbox from Altera. DSP Builder allows to do the project and simulation of digital signal processing systems for Programmable Logic Devices (PLD) in Simulink software from MathWorks. The simulations of the digital demodulator were done using tool Hardware in the Loop (HIL) from DSP Builder. HIL tool programs a Programmable Logic Device (PLD) with a desired project including an interface for communication with the PC that allows simulate it in the Simulink environment. The communication between the hardware and the PC is done by a JTAG cable. This kind of simulation gives the advantage of using the Simulink and Matlab library for stimulus generation and signal analysis, and is very fast since the signal process is realized by the hardware.

A model of the received signal was generated in Simulink, based on the characteristics presented on section 2. White noise was added for better representation of the real case signal, and a sample time of 10ns was used, as in the A/D output. This model was used to generate the input for the simulation. Figure 6 shows this model and fig. 7 the simulation scheme using HIL.

The Signal to Noise Density (S/N_0) of a BDCS signal at the NI-PXI 5600 output of the EMMN ground station varies between 30 dB to 18 dB. This was measured with a spectral analyzer. Here we present two simulations with different S/N_0. The first simulation was with low noise, S/N_0 of 30 dB at the carrier frequency, to compare the modulator signal with the demodulator signal in time domain. Fig 8 shows the modulator input (PCDs.mat) followed by the DPLL output.

The second simulation was with S/N_0 20 dB. We can see, analyzing the loop filter accumulator, that the loop locked at the right frequency (figure 9a), but the linear range limit of the phase detector is exceeded, causing error in the demodulated signal (figure 9b). Figure 10 shows the FFT of the input modulated signal.

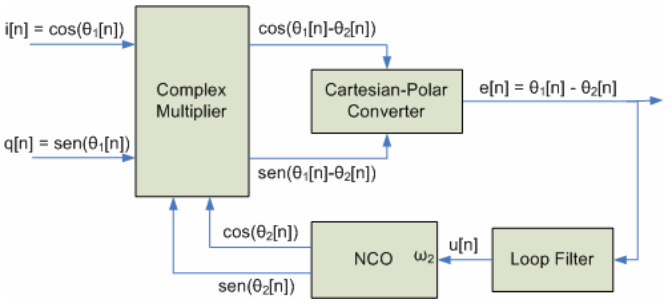


Figure 5. Digital phase locked loop architecture.

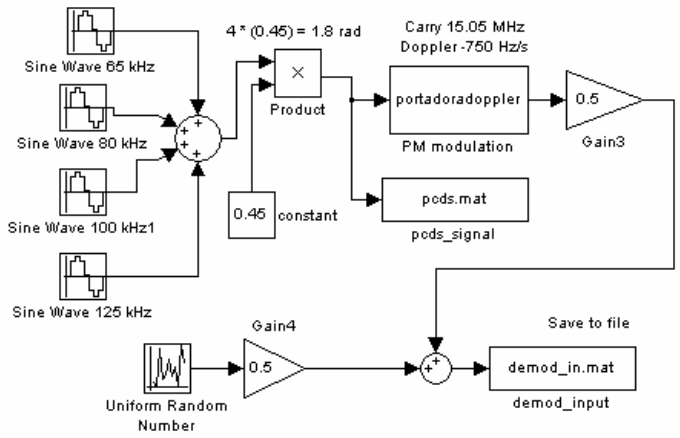


Figure 6. Simulink model of BDCS satellite signal.

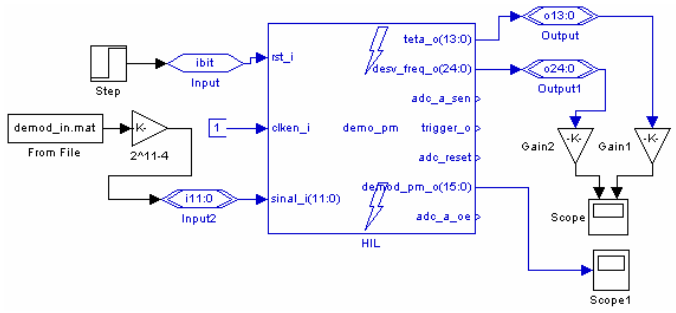


Figure 7. Project simulation using HIL function

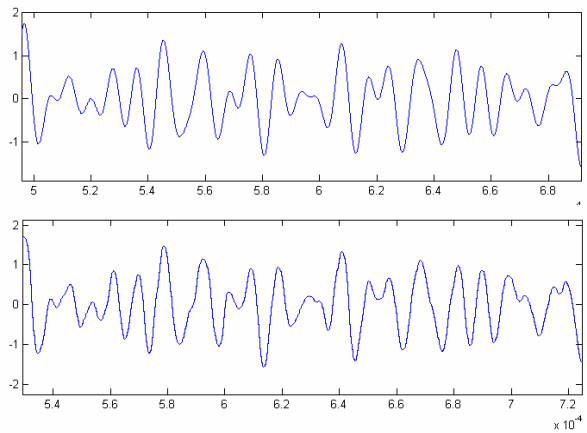
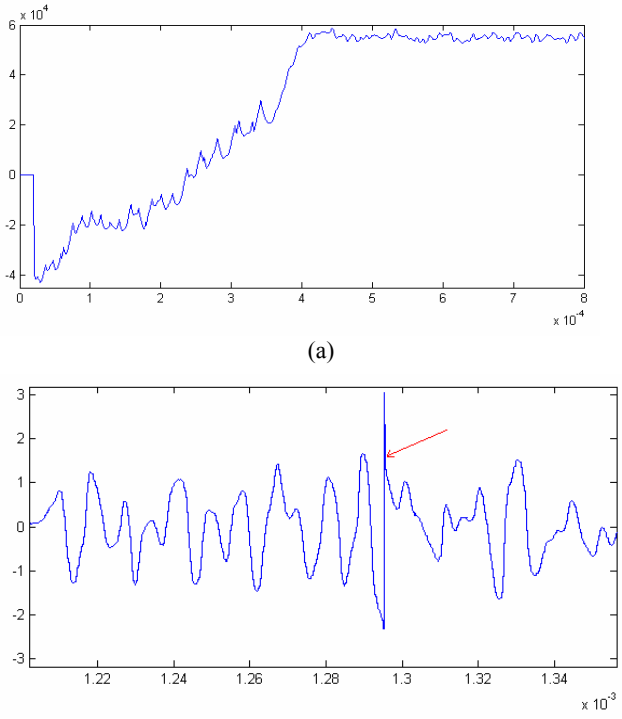


Figure. 8. Above modulator signal and bellow DPLL output. S/N_0 of 30dB at the carrier frequency



(a)

(b)

Figure. 9. a) loop filter accumulator output in Hz; b) part of the demodulated signal showing the linear range limit of the DPLL being exceeded.

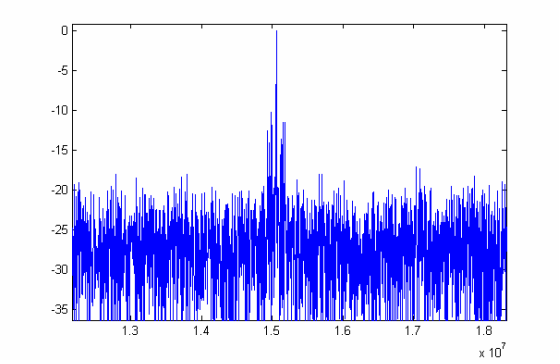


Fig. 10. Modulated signal FFT

7. CONCLUSIONS AND FINAL CONSIDERATIONS

The simulations demonstrated that the demodulator works as expected, but improvement can be made since the linear operation limit of the DPLL is being exceeded when S/N_0 level is lower than *20 dB*, that is, when there is too much noise. Possible solutions to improve the performance of the DPLL with noise input are to use a more complex architecture as a dual loop PLL [4] or use a second order Loop Filter [5].

To finish the project it is also necessary to implement the communication circuit between demodulator and PC. This should transfer 390 KSPS with a 16 bit word sample. A possible solution is to use USB v2.0 protocol to make this communication.

8. ACKNOWLEDGMENTS

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